SPICE – THE FOURTH DECADE
ANALOG AND MIXED-SIGNAL SIMULATION – A STATE OF THE ART

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SUMMARY

This paper describes the challenges facing analog designers today and the progress of EDA capabilities towards this need. The recent developments are presented as an evolution from a single analysis tool, the Berkeley SPICE simulator to the multitude of analog simulation and characterization tools.

1. INTRODUCTION

The SPICE program [1], [2], has been the principal design tool for analog and digital circuits for three decades following its initial release in 1970 under the name CANCER [3]. Even today SPICE remains the main electrical verification tool for such complex custom designs as microprocessors and memories.

The first section summarizes the evolution of this standard from its initial research at the University of California at Berkeley [4], [5], [6], [7], to its current many commercial implementations[8], [9].

The second section highlights Integrated Circuit, IC, technology developments which have been and are the main driver for advancing the state-of-the-art of Electronic Design Automation, EDA, tools.

The next two sections contain an overview of the recent advancements in the two main areas of expertise of a circuit simulation program, algorithms and device modeling.

Extensions of the coverage area of circuit simulation into digital as well as other physical domains and higher levels of representation than the transistor are described in sections 5 and 6.

A last section is dedicated to future developments.

2. SPICE – THE FIRST THREE DECADES

The continuing development and improvement of SPICE since its early days in the late 1960s has taken place in the two general areas which are integral parts of the simulator: algorithms and device modeling.

Initially, algorithmic research took first priority and by the end of the first decade of its existence SPICE benefited from a set of stable and accurate solution algorithms commonly referred to as *direct methods.* The sequence of implicit numerical integration of ordinary differential equations, ODE, modified Newton algorithm for the solution of nonlinear equations, and, LU factorization and solution of sparse systems, constitute of direct methods and the core of any SPICE program.

By the start of the 1980s, the second decade, SPICE had been adopted by most IC companies as their standard for design and verification. Increasing importance was given since the latter part of the 1970s to the accuracy of semiconductor device models. The initial Ebers-Moll [10] bipolar and Shichman-Hodges [11] quadratic MOSFET models present in the first versions of SPICE were updated with an extended Gummel-Poon [12] model for BJTs and a physical and semi-empirical MOSFET models, known as LEVEL 2 and 3 [13]. While the BJT model held up well through the 1980s due to its unique and continuous formulation across all regions of operation the fragmented formulation of the MOSFET equations by operating region plagued the LEVEL 2 and 3 models despite their inclusion of most second-order physical effects observed in small-size devices [14], [15]. These shortcomings along with the need for ever-increasing accuracy led to a renewed emphasis on device modeling in the 1990s as detailed below.

In the 1980s emphasis was also placed on ease of use and robustness of the solution algorithms. The former was helped by the introduction of minicomputers, engineering workstations, personal computers, interactive operating systems such as Unix, and, Electronic Design Automation, EDA, software. The latter, simulator robustness, was the result of many parallel efforts in universities, dedicated CAD groups of semiconductor and system companies and EDA companies offering proprietary

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versions of SPICE integrated in their design software.

By the end of its second decade in existence, the late 1980s, SPICE was not only the standard for IC design but was robust enough that in the words of some experienced analog designers, convergence not only ceased to be a simulation problem but became an indicator of probable design problems.

The next section takes a closer look at the technology drivers and SPICE simulation developments in the current decade.

3. TECHNOLOGY GENERATIONS AND DESIGN

Technology scaling and the resulting increase in functionality implemented on a single chip led to a series of advances in circuit simulation on all fronts: algorithmic, device modeling and functionality extensions into related fields such as digital on one hand, and, related physical domains, such as mechanical, on the other.

Moore's law remained valid during this decade, the number of transistors per chip kept increasing fourfold every three years; four device generations have been introduced into production this decade, from 0.5μ down to 0.18μ; the number of interconnect layers has gone from 4 to 7. These developments have far-reaching implications on IC design beyond the obvious single device physical behavior.

First, the bandwidth of transistors has increased to the point where RF circuits can be built using standard IC technology which combined with reduced power consumption puts a single-chip radio within reach. IC design methodologies have pushed into the realm of RF design and therefore SPICE simulation with its established functionality for nonlinear circuits had to be adapted to this field.

Second, the average length of intermediate and global interconnect keeps increasing invalidating the assumption of a perfect conductor. This issue was approached from several points of view, the digital perspective, linear *rlc* network and analog simulation. These approaches are detailed in a later section on interconnect.

Third, the complex functionality that can be implemented on a single chip needs a way to describe the system rather than the circuit leading to the introduction of standards for analog and mixed-signal description languages.

4. ALGORITHMIC DEVELOPMENT

While the major emphasis in the 1980s was placed on finding alternate, faster, algorithms to the direct methods approach used in SPICE [16] to solve the time-domain response, the research in the 1990s concentrated on new algorithms to extend the functionality of SPICE simulators. At the same time more fine-tuning was brought to the existing algorithms in order to insure robustness of simulation of circuits with tens of thousand of transistors. These developments are described in the subsections below.

Circuit Simulation Robustness

The main algorithms of SPICE although robust at the beginning of this decade were strengthened with the automation of continuation methods for the DC solution and the fine-tuning of the truncation error and time-step control algorithm in the time-domain solution. State-of-the-art commercial SPICE simulators such as Spectre [9], HSPICE [8] and Eldo [17] offer these improvements.

Improved DC convergence reliability results from using source ramping, conductance ramping and transient ramping for finding the DC solution automatically by the simulator when the standard approach to DC [1] fails.

Robust transient is addressed by effective ways of sensing the rate of change in circuit variables over time and adjust the time step for best accuracy and stability of the integration method used.

All above simulators offer encapsulated sets of analysis options for the nonlinear equation solution and numerical integration classified as liberal, moderate or conservative, or, standard and accurate, for less experienced users. These global selections combine convergence-tolerance values with integration methods and truncation-error tolerances which the user must choose based on the characteristics of the circuit. Although this facility takes some of the guesswork related to each individual analysis option it still leaves the user the responsibility to judge the level of accuracy needed for each circuit or class of circuits.

Steady-State and RF

Steady-state solution of nonlinear circuits has been a topic of research since the early days of circuit simulation. While a number of research projects were dedicated to this topic over the decades [18], [19], [20], few commercial simulators offered such an analysis and even the ones that did, like MDS [21], were mostly limited to linear circuits.

Until few years ago the only viable approach to obtain a steady-state solution was harmonic balance [22], [23], [24]. Harmonic balance assumes that signal variables are formulated as Fourier series and solves for the different-order coefficients in the frequency domain. While this works very well for mostly linear circuits with distributed elements, the

Harmonica/Spectre project [19] at UC Berkeley showed that the higher the circuit nonlinearity the less efficient this method becomes.

The advance of IC technology into the RF application area raised the importance of accurately simulating transceivers which are very common in communication circuits. The problem arises when simulating the difference signal IF, typically in the range of tens of kHz to tens of MHz, obtained from mixing the incoming RF signal with a local oscillator LO, both signals in the GHz range. The traditional SPICE transient analysis would be prohibitively expensive having to follow the highest-frequency signal.

The goal for a number of research projects [18], [20], has been to find a solution to this problem in the time domain. It is straightforward to describe device nonlinearities in the time domain and having a time-domain steady-state solution has the advantage of obtaining the transient solution, e.g. oscillation build-up, as part of the same process. Newton shooting methods have held the most promise but it was not until its implementation in SpectreRF [9] that this algorithm was applied successfully to more divers classes of circuits such as mixers and oscillators.

The shooting method is an iterative procedure layered on top of a transient solution which is meant to solve the boundary constraint $v(T)-v(0)=0$ for a circuit driven only by periodic inputs. The results of this analysis can then be viewed both in time domain as well as in frequency domain. The steady-state solution of a periodic circuit is equivalent to the operating point of a time-invariant circuit. Extending the operating point concept to time-varying circuits has beneficial extensions to small-signal analyses. Since operation of communication circuits often involves several signals of different frequencies and amplitudes, some signals can be considered small compared to one large-signal for which the steady-state solution has been obtained; then, a number of important characteristics such as conversion gain, intermodulation intercept and noise figure can be obtained through a very fast small-signal analysis [25].

Envelope simulation [26], overcomes the limitations of harmonic balance by extending the Fourier coefficients to include time dependency, or, put differently, it takes input stimulus as RF carriers with time-varying complex envelopes. Similar to shooting methods envelope simulation does not concern itself with the carrier signal, included in the harmonic balance solution, but with the modulating, slow moving, signal; therefore, the time-step of the numerical integration method needs to follow only the latter signal. The new ADS simulator [29] implements this algorithm and it can also be used successfully to characterise mixers and amplifiers under multi-tone sinusoidal excitations, or, settling times of a voltage-controlled oscillator, VCO.

Interconnect

The increasing importance of interconnect characterisation for reliable verification of functionality and performance both at chip and board level has triggered a new research topic related to analog simulation. This new research targets effective algorithms to solve the complexity of the linear network resulting from a two- or three-dimensional extraction of the interconnect. The Asymptotic Waveform Evaluation, AWE, algorithm based on Pade approximation [27] has been a successful approach of approximating a Laplace-domain transfer function of a linear network by a reduced-order model, containing a reduced number of poles and zeroes depending on the desired accuracy. Such a reduced-order model can then be used in a SPICE program for an effective simulation of the nonlinear circuit including the interconnect. The original AWE algorithm suffered from numerical accuracy problems when more than a few poles or zeroes were required. This is a topic of continuing research; one algorithm which has been shown to be numerically stable and capable of generating an arbitrary number of poles and zeroes for the reduced model is Pade via Lanczos, PVL [28].

A different approach to include the effect of interconnect into circuit verification was adopted in the digital arena. While digital simulation ignores the effect of interconnect both from the point of view of delay as well as propagation characteristics it became imperative first at the board level that transmission-line effects, and, driver and receiver characteristics must be considered. A new set of tools and modelling approach were developed known as Signal Integrity tools and IBIS models, respectively. The former include electric field solvers for extraction and linear network solvers, and, the latter are I-V tables which map the nonlinear characteristics of drivers and receivers. At the chip level, for ASICs, most interconnect is only considered as part of timing verification; for state-of-the-art custom designs, such as processors or memories, SPICE-level simulation is still the norm.

5. SEMICONDUCTOR DEVICE MODELLING

Semiconductor device models are as important to the accuracy of simulation as are the underlying simulation algorithms. This is the reason for continued interest in this field; the technological

progress listed above make it imperative to revisit and update simulation models to match the behaviour of ever-shrinking transistors.

Several important developments took place in the latter part of this decade.

First, and foremost, a decided push towards standard, public-domain models has been winning the contest over proprietary device models. Proprietary models are tied to a specific simulator constraining the user to this one simulator; investments in process characterization, collaboration among different design groups as well as with foundries have been the main contributors to tilting the balance in favour of public-domain models.

Second, after almost two decades of satisfying most needs for bipolar transistors, the Gummel-Poon, GP, model came under scrutiny. Shrinking device sizes in BiCMOS and RF bipolar processes highlighted shortcomings of the GP model related to the distributed nature of the base and collector, quasi-saturation, base-doping profile, depletion-charge modelling and temperature effects. The two models which include these effects, the Philips MEXTRAM [29] and VBIC [30] model have experienced wider use. Both models are in the public domain and are implemented in the top commercial SPICE simulators.

Third, MOSFET models with a continuous formulation over the three regions of operation, subthreshold and strong inversion, linear and saturation, have been introduced. There are currently three submicron MOSFET models which lead in accuracy: BSIM3v3 [31], EKV [32] and Philips MOS9 [33]. While none of the three has solved the fundamental problem of developing a unique analytical formulation for all regions of operation, all use smoothening functions which provide adequate continuity of the conductance g_{ds} and transconductances g_m and g_{mbs} of the device.

Fourth, efforts are underway to develop models for Silicon-on-Insulator, SOI, devices which may replace the surface-channel MOSFET for further miniaturisation. One such effort led to BSIM3v3 models for partially-, fully- and dynamically-depleted devices. An important challenge of modelling and simulating these devices is the floating body terminal.

Fifth, high-frequency models have gained in importance for RF designs. The challenge here is to replace tables of *S* or *Y* parameters formerly used in RF design due to their limited validity to operating conditions by a compact model, as in mainstream IC design. A BSIM3v3-RF model has been found to accurately model the behaviour of MOSFETs in the GHz range. Additionally, accurate representations of microstrip lines are now present in most SPICE simulators to model the impact of interconnects.

6. ANALOG HARDWARE DESCRIPTION LANGUAGES

The need to verify proper operation of larger components or systems, the interface between analog and digital, or, electronic sensing and control of mechanical parts, have driven the development of a standard description language. There are many situations when only a behavioural definition, e.g., input/output equation of a component is known or relevant. Many physical systems can be described in terms of ODEs for which SPICE is an excellent solver. Already before introducing any high-level specification capability SPICE had been used in other application areas like mechanical engineering through equivalent electrical macromodels described in SPICE netlist language which is a standard in its own.

Although specification languages for circuit simulators had already been introduced, e.g. ASTAP, MAST, these languages could be used with just the simulator for which they had been developed, i.e., ASTAP and Saber, respectively. Model development represents an important investment and designers wanted the flexibility to carry this investment from one simulator to the next when new functionality became available. This led to establishing two new standards, Verilog-AMS [34] and VHDL-AMS; they are based on the corresponding digital languages enriched with the constructs needed for analog and physical systems.

Another approach to high-level modelling was taken by Profile [35], a graphical/textual, block-diagram interface which combined portability with ease of use. The block-diagram is fed through a translator to a SPICE simulator supporting arbitrary-equation processing. Profile is similar to other simulation interfaces like Ptolemy [36], or Simulink [37], where the diagram provides the connectivity information and the behaviour is obtained straightforwardly from the underlying equations.

```
module vco(in,out)
  input in;
  output out;
  node (V,I) in,out;
  parameter f_ref, Kv;
  real freq, phase;

  analog begin
     freq = f_ref + Kv*V(in);
     phase = integ(2*PI*freq);
     V(out) <- sin(phase);
  end

endmodule
```

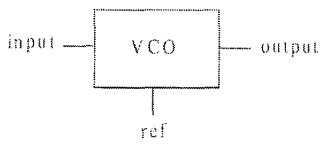

Figure 1. Behavioural model of VCO in Verilog-AMS

The example shown above in Figure 1, illustrates how a VCO could be introduced as a black box into simulation its functionality described only with reference to its three terminals, input, output and ref. This block can be simulated with transistor-level circuitry as well as other high-level blocks which can be defined both in time- or frequency domain. The most common circuit simulators today support at least one of the two new standards.

7. BEYOND JUST ANALOG: MIXED-SIGNAL

There are many applications which combine analog and digital processing. Examples include control applications, signal processing, power electronics, etc. In the first application a microprocessor takes input data from analog circuits, processes the information, and issues control decisions to more analog circuits. The digital processing part of communication channels or multimedia applications is also more complex than the analog part but the issues of interest differ from the first example and a different computational may be necessary to simulate its behaviour.

Another aspect of mixed-signal issues are represented by digital circuits which need to consider analog transmission effects such as signal reflection and crosstalk in their design.

The typical solution to the mixed-signal problem offered by industry and universities has been to interface a SPICE simulator to a digital simulator and synchronize the two time queues. Very few circuits have been designed successfully with these tools. The successful design tools in this realm have been those which addressed a specific application such as the Signal-Processing Worksystem, SPW, from Cadence or Matrix-X from Integrated System Inc. for control applications. Although useful, these tools lack the accuracy of a SPICE-type solution for analog components which are part of the system; there is no link or valid alternative to a nonlinear analysis. .

The Ptolemy [44] project from UC Berkeley tried to address this issue by offering an environment and synchronization engine where different models of computation can be plugged in. Ptolemy works very well for signal-processing applications and has recently been used also for reactive and real-time systems; it has not been used to cover several levels of accuracy down to the transistor level.

A platform which has gained wide acceptance as a platform for implementing and experimenting with different solution algorithms at different levels of accuracy is MATLAB. Its system-level capability SimuLink, fashioned after Ptolemy, has a hierarchical block-diagram schematic tool where each block can be assigned a simple or complex mathematical behavior, and then, can be simulated in time-domain. SimuLink has been successfully used to design a multi-user CDMA communication channel with both analog and digital components. The missing link however is the path from this higher level down to the hardware implementation. These are remaining challenges.

8. CONCLUSION, FUTURE DEVELOPMENTS

In this decade SPICE simulation technology has become mature; some of the missing functionality such as steady-state analysis and support for general description of components has been added. While the robustness of the SPICE simulators is high the opening up of the simulator to model development by the user at large may pose some challenges.

The main challenge for the next few years is to develop the verification tools for analog and mixed-signal systems rather than circuits. It is clear that the SPICE-level solution is essential and as such will be a part of a future system verification capability. Network reduction algorithms, fast linear equation solvers as well as integrated digital simulation need to supplant the SPICE solution.

It is expected that a designer would have a unique description of the hardware with combined analog and digital blocks; this unique description will have to be simulated by a single tool which depending on the description would need to decide the level of accuracy and speed to be applied.

System design will take place mostly in a Simulink/Ptolemy-type tool and there will be a need for automatically linking to the hardware implementation: bringing in pre-characterized analog circuit blocks, synthesize the digital piece and verify the implementation.

The complexity of designs and explosion of resulting analysis data require the development of smart output processors which can help interpret and compare performance with respect to objectives.

For the next decade SPICE in its different commercial implementations will still be the standard for analog simulation. It is conceivable that circuits with a few hundred thousand devices could be simulated by the end of the next decade if the engineering workstation performance continues to increase according to Moore's law. It is also important to note that the SPICE solution algorithms will be embedded or linked to the verification tools which will support system-level design.

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