ECE 521 Fall 2016

Homework #3 - Part 2 (Due Nov 7)

In this HW you will **extend** *myspice* to **solve** a system of **nonlinear equations**, i.e., perform **dc analysis** of nonlinear circuits. You have already implemented the Newton iterative loop in HW# 2.

a) Add the code to **readin**, **setup**, and **load** *diodes*. The syntax is

```
Dname node(p) node(n) model value <the area field>
```

The diode is described by $I = Area \times I_S \left(e^{\frac{V}{V_T}} - 1 \right)$ where $I_S = 1 \times 10^{-16}$ A, $V_T = 0.0258$ V. You do not have to implement a model "readin" and processing and can hardcode the parameter values (I_S and V_T).

b) Solve the circuits test[9-10].ckt using *myspice* and note the number of iterations to convergence.

c) Modify the diode stamping such that *pnjlim* is used for limiting the diode voltage before calculations and stamping. The *pnjlim* function from Spice3 is provided. Rerun test[9-10].ckt. How is the convergence of these examples with limiting?

d) Add the code to **readin**, **setup**, and **load** *MOSFETs*. The MOSFET syntax is

```
Mname node(d) node(g) node(s) node(b) model value value <W and L, respectively>
```

The equations describing a NMOSFET are

$$I_d = \begin{cases} k' \frac{W}{L} \left[(V_{gs} - V_T) V_{ds} - \frac{{V_{ds}}^2}{2} \right] (1 + \lambda V_{ds}) & V_{gs} \geq V_T, V_{ds} \leq V_{gs} - V_T, \text{ linear} \\ \frac{k'}{2} \frac{W}{L} (V_{gs} - V_T)^2 (1 + \lambda V_{ds}) & V_{gs} \geq V_T, V_{ds} \geq V_{gs} - V_T, \text{ saturation} \\ 0 & V_{gs} < V_T, \text{ cutoff} \end{cases}$$

$$V_T = V_{TO} + \gamma \left(\sqrt{V_{SB} + \phi} - \sqrt{\phi} \right)$$

The following parameters should be used

n-ch: $V_{TO} = 0.7$ V, $k' = 100\,\mu A/V^2$, $\lambda = 0.05\,V^{-1}$, $\gamma = 0.5\,V^{1/2}$, $\phi = 0.6$ V

p-ch: $V_{TO} = -0.9$ V, $k' = 50\,\mu A/V^2$, $\lambda = 0.05\,V^{-1}$, $\gamma = 0.5\,V^{1/2}$, $\phi = 0.6$ V

You can hardcode these values (and not implement a model) but must distinguish between a NMOSFET and PMOSFET using the model field that is NMOS or PMOS, respectively. A template is included (mosfet.c, mosfet.h) for the MOSFET load. This is not functional code for *myspice* but is a template for writing the MOSload function with appropriate modifications. **The derivatives, current calculations, and stamps in this template are correct!**

e) Solve the circuits test[11-16].ckt using *myspice* and note the number of iterations to convergence. List any convergence improvement techniques you had to use to get these circuits to converge. The code for the Spice3 limiting functions *limvds* and *fetlim* is provided.

f) Add the code to **readin**, **setup**, and **load** *NPN BJTs*. The syntax is

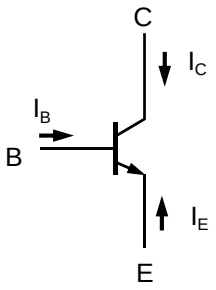
```
Qname node(c) node(b) node(e) model
```

The equations describing a NPN transistor are

$$I_C = I_S\left(e^{V_{BE}/V_T} - 1\right) - \frac{I_S}{\alpha_R}\left(e^{V_{BC}/V_T} - 1\right)$$

$$I_E = -\frac{I_S}{\alpha_F}\left(e^{V_{BE}/V_T} - 1\right) + I_S\left(e^{V_{BC}/V_T} - 1\right)$$

$$I_B = -(I_C + I_E)$$



The following parameters should be used
$V_T = 0.0258$ V, $I_S = 1\times10^{-16}$A, $\alpha_F = 0.99$, $\alpha_R = 0.01$

You can hardcode these values (and not implement a model). Use *pnjlim* for limiting the forward biased junction voltages before calculations and stamping.

g) Solve the circuits test[17-18].ckt using *myspice* and note the number of iterations to convergence.