Hands-on Homework 3: Reflections on Finite Length Lines

Introduction

Reflections that occur on transmission lines can be used to help create proper signaling conditions at a receiver or can disrupt the receiver input. We can tailor transmission line terminations to create the conditions we want. In the AC domain, we can even make the transmission line look like a particular reactive element at particular frequencies. In this exercise, we will observe three terminating conditions and the reflections they may or may not produce.

In each of three conditions, we drive the transmission line from a pulsed source with a source terminating resistance that is matched to the line impedance; in this case 50 ohms. This is actually a commonly used circuit configuration often called a *source terminated* transmission line, as its only termination is at the source. This is a simplifying construction that prevents a reflection from ever originating from the source end. For now, we want to focus only on reflections from the far or receiver end.

The first case we will look at is shown below. The line is driven from the source terminated driver. The far end is left open circuited. The discontinuity at the open circuit end requires that a positive reflection return back towards the source so that KCL may be obeyed. See Figure 1.

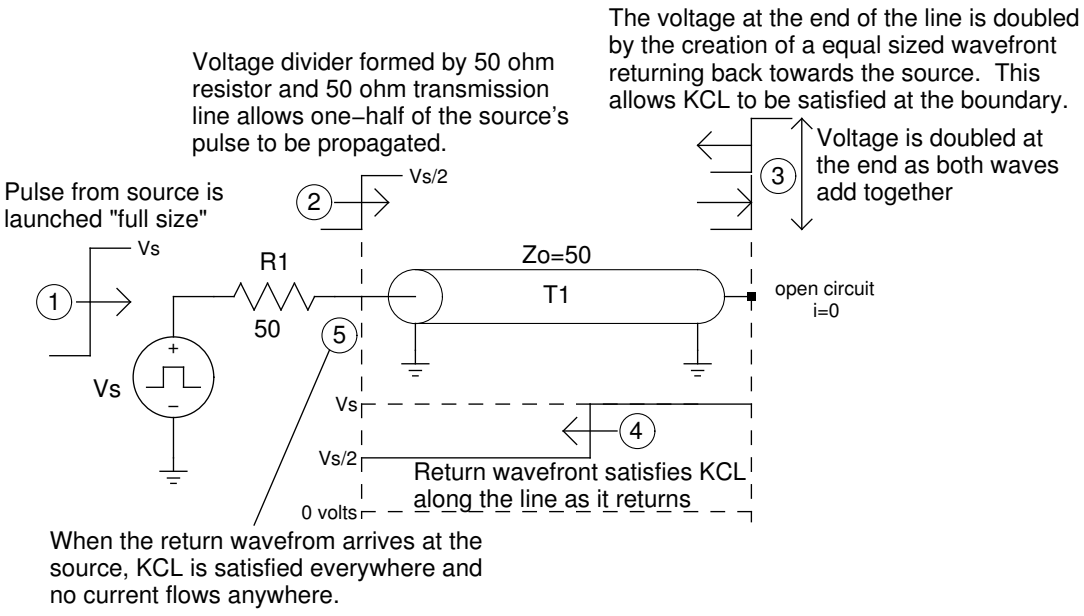


Figure 1: Source Terminated Transmission Line

Building the circuit below, we can duplicate the theoretical results. Refer to the schematic in Figure 2.

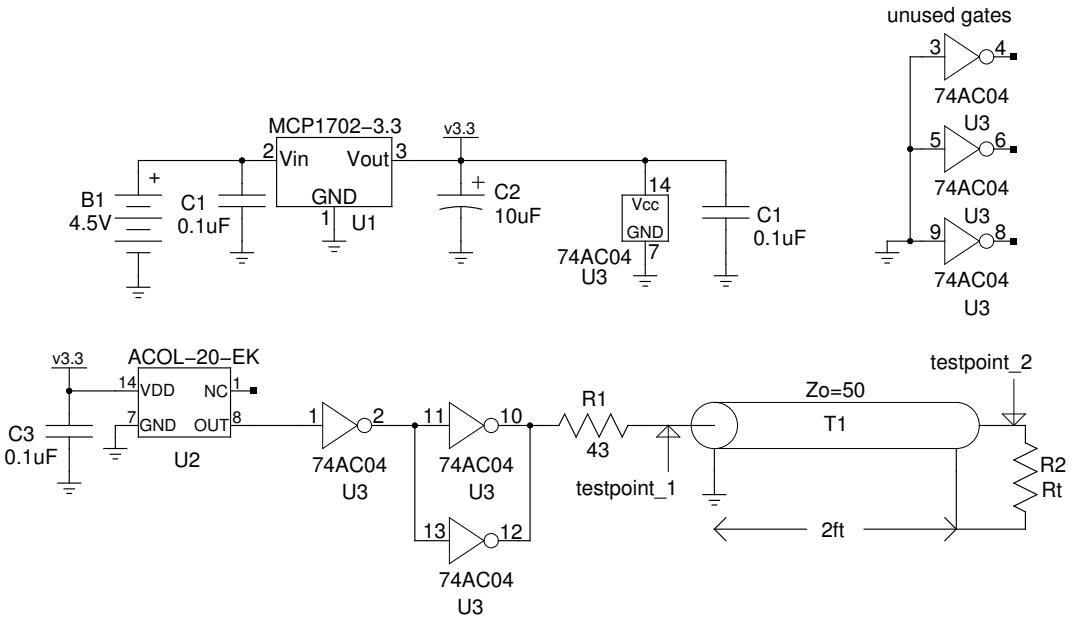


Figure 2: Schematic Diagram

This circuit is the oscillator circuit we had before plus a hex inverter, the 74AC04, and a length of coax cable. The inverters, which are driven from the oscillator, forms our pulse source. A two foot length of RG-174 coax cable serves as the transmission line.

Now, for some explanation of the circuit. The unused inverters in the 74AC04 have their inputs tied to ground. This is to prevent their inputs from *floating*. If the inputs are allowed to float, the input voltage settles to one-half the supply voltage which is typically the switching threshold. Right at the switching threshold, both N and P output transistors are on, providing a path from Vdd to Ground. This causes considerable power is drawn by the inverters. Good engineering practice is to *always* tie unused CMOS inputs to either power or ground.

The first section of U3 drives two inverters in parallel. This is done to lower the output impedance driving the coax cable. A single 74AC04 inverter has an output impedance of about 14 ohms. The output impedance of the inverters originates from the Rds(on) resistance of the P and N channel MOSFETS in the inverter output stage. Two inverters combined provide an equivalent 7 ohm output impedance. This allows R1, the source terminating resistor to be the dominant component in determining the source terminating value.

You may note a fairly free interchanging of the terms resistance and impedance above. In reality, the inverters have both a resistive and reactive component to their outputs. However, in our application, the reactive component is so small it can be largely ignored. This would not be the case at higher frequencies or edge rates.

R1 is a 43 ohm resistor. Its value is set so that the combination of inverter output impedance and R1 form a 50 ohm resistor. The equivalent circuit for our driver would be a voltage source and a 50 ohm resistor just as the theoretical model is. Rt, at the end of the line is for the present

experiment infinite. We simply leave the end of the coax cable open circuited.

The shield of the coax is shown connected to ground at its driven end. However, the path through the inverters to ground is not so clear. In fact, the only ground for the inverters is shown near the voltage regulator. It is typical for digital circuits to show all power and ground connections elsewhere to prevent cluttering the schematic with power wiring. Our circuit is digital, but the behavior we are interested in, is analog. To make the current paths clearer let's digress a moment. See the schematic in Figure 3.

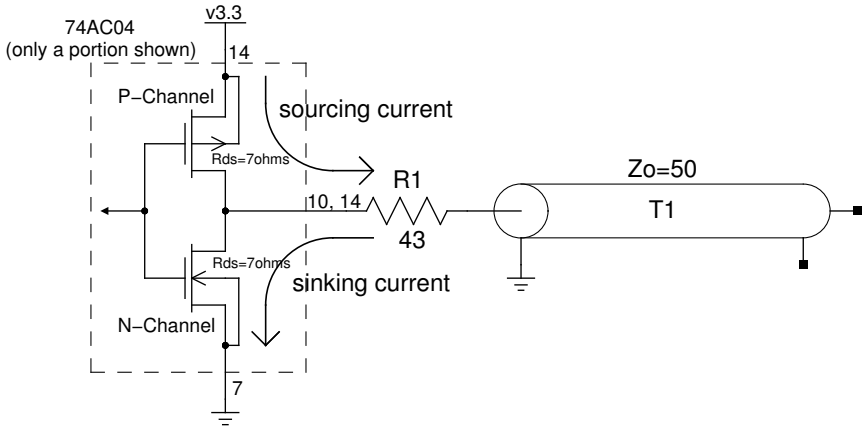


Figure 3: Output Buffer Current Paths

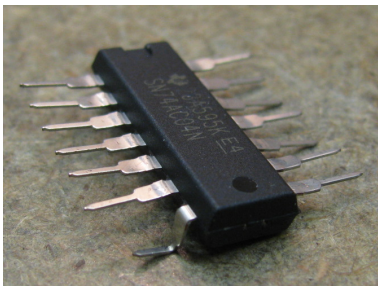
When the inverter supplies current to the transmission line, as when launching a rising edge, it *sources* current from the 3.3 volt supply, through pin 14, through the P-Channel transistor, to the transmission line. This top transistor, here representing the output transistor in the two paralleled inverters, has an output impedance of about 7 ohms.

Its mirror image, the N-Channel transistor, supplies the path for current to be drawn from the transmission line such as when a falling edge is launched. When *sinking* current, the N-Channel transistor provides the path to ground through the pin 7. The resistance through the N-Channel transistor is also about 7 ohms. From this schematic, you can see that the function of the two transistors in the output stage is to connect downstream circuitry to power or ground.

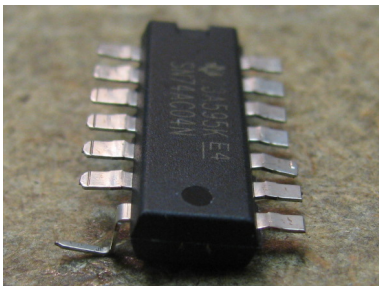
Building the Circuit

Using the existing oscillator circuit on your PCB, add the 74AC04 and associated components using ugly construction. You may need to reclean the area where the 74AC04 is mounted. Solder the ground pin of the 74AC04 first and then add the decoupling capacitor. This way, the chip will stay put while you add the capacitor. The other pins on the IC are are bent straight out and the thin part of the pin is clipped off. This leaves a wide area for soldering to.

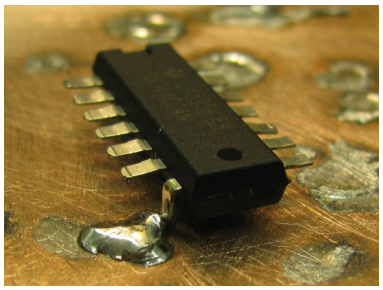
Ground the unused pins with separate wires to ground so the inverters may be reused if needed without unsoldering pins attached to the PCB. Refer to the manufacturers data sheets for package and pin orientation. Keep all signal leads as short as is practical. You can coil up the coax if you wish to keep in under control. You may ground the shield on the far end if you wish to



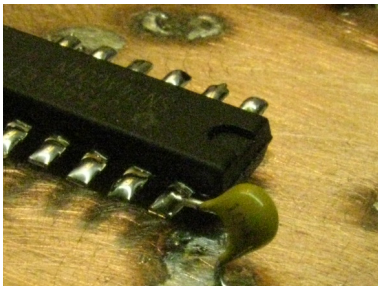
(a) IC with Legs Bent



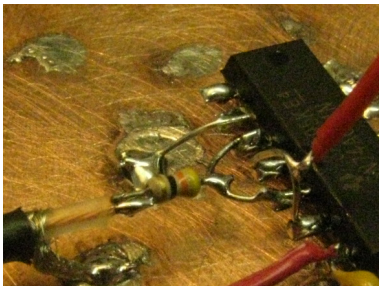
(b) Legs Bent and Clipped



(c) Ground Pin Soldered



(d) Decoupling Cap Soldered



(e) Coax/Source Termination

(f) Completed Circuit

help you probe the cable end. The signal return path will not use the PCB ground plane but will instead travel along the inside of the cable shield.

Circuit Measurements

Power up the circuit and connect one scope probe to testpoint_1 and the other to testpoint_2 using short ground leads for both probes. Set the scope to trigger on the rising edge of the waveform at testpoint_1. A trigger level of 0.75 volts should be fine. Set the display to show both channels and the clear waveform "step" at the testpoint_1. If your setup is roughly correct, you should see something as shown below.

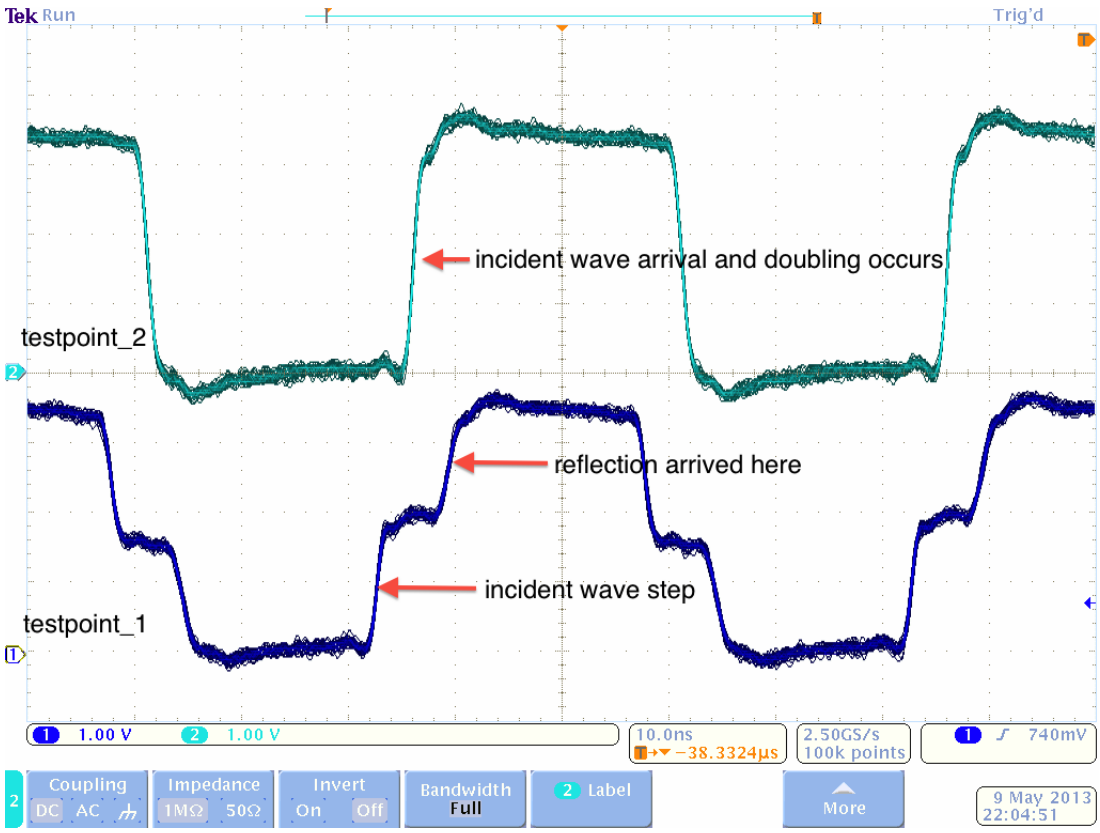


Figure 5: Source Termination, Far End Open Circuit

1. Capture an oscilloscope picture of the rising $Vdd/2$ edge at testpoint_1 and the corresponding doubled waveform at testpoint_2. You will need to zoom in far more than shown above so that you can make a measurement with the cursors to determine the time delay from the initial rising edge at testpoint_1 to when the reflection returns at testpoint_1 and it rises to Vdd. Include this picture in your report.

2. Find the velocity of propagation for RG-174. Show by calculations and written explanation that the delay from the initial edge at testpoint_1 to when it completes rising to Vdd is consistent with a 2ft piece of RG-174.

3. Capture an oscilloscope picture showing a cursor measurement of the voltage of the initial Vdd/s step at testpoint_1 and the Vdd doubled wavefront at testpoint_2. Was the choice of a

43 ohm resistor about correct? How can you know by what your voltage measurements tell you? Include the answers to these questions and this scope picture for your report.

When the reflection from a transmission line discontinuity, such as the open-circuited line, is as large as, and is of the same polarity as the incident wave we say that the discontinuity has a *reflection coefficient* equal to one. The symbol "rho" ρ is used to indicate the reflection coefficient. For this case we would say that $\rho = 1$.

Now we will look at another scenario where the amplitude of the reflection from the far end of the transmission line (the discontinuity) is equal to amplitude of the incident wave but is negative in polarity. So for this circuit, $\rho = -1$. This circuit configuration finds very little application but does provide insight as to how and where negative reflections occur. See Figure 6.

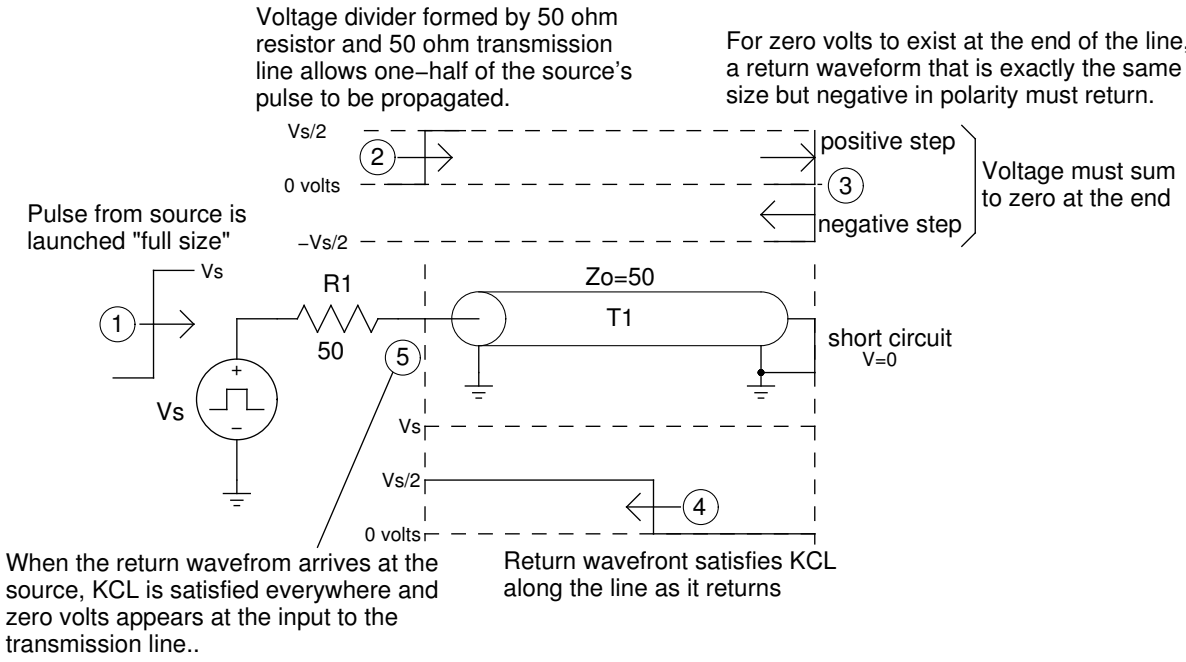


Figure 6: Source Terminated, Shorted End Transmission Line

Again, we drive the line from the source terminated driver. However, the far end is short circuited. For zero volts to exist at the far end when a positive wavefront arrives requires that a reflection be produced that is equal but negative in value to the incoming wavefront.

For this circuit, we need only probe testpoint_1. As before, set the scope to trigger on the rising edge of the waveform at testpoint_1 with a trigger level of 0.75 volts.

Warning: This experiment draws a large amount of current from the batteries and strains the voltage regulator. You need to take your measurements quickly. Get your setup running without the short first. Then briefly short the end of the line and take the scope picture. Then remove the short or the power.

When your setup is correct, you will see a signal similar to that shown below.

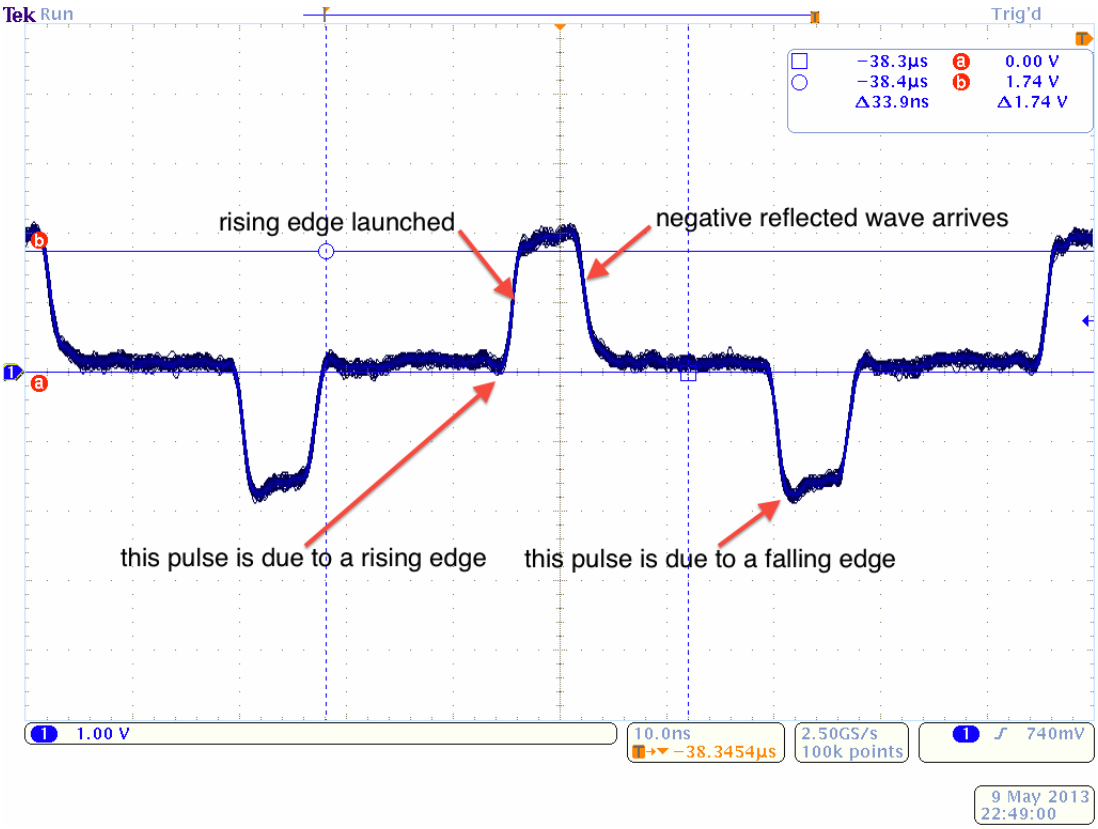


Figure 7: Waveforms at testpoint_1 with Shorted Far End

4. Make a measurement with the cursors to determine the width of the positive pulses. You will need to zoom in more than the picture above. Capture an oscilloscope picture of your measurements.

5. Using the velocity of propagation for RG-174, show by calculations and written explanation that the pulse widths you see are consistent for a 2ft piece of RG-174.

The last scenario is where the reflection from the far end of the transmission line is zero. Thus $\rho = 0$. This situation occurs when the far end of the transmission line is terminated in its characteristic impedance. See Figure 8 below. The current which a wavefront causes to flow continues to flow at the end of the transmission line due Rt being a 50 ohm resistor. To the wavefront, the resistor appears as a infinite length of 50 ohm transmission line. So there is no discontinuity at the line end and no reflection is required.

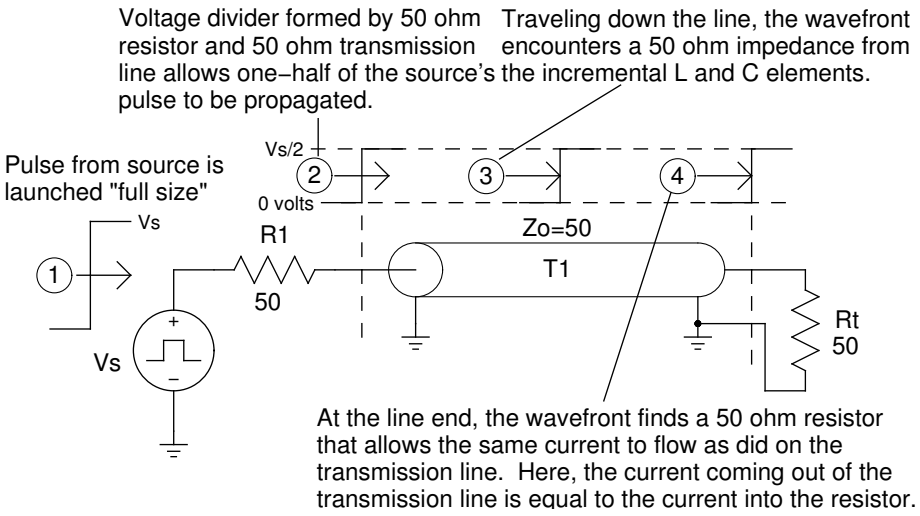


Figure 8: Source Terminated, Zo Terminated Transmission Line

This termination style is often called *double terminated*. It is sometimes used for video applications where reflections must be absolutely minimized. However, the signal at the far end is only half of what was initially transmitted. As such, you find that many video buffers (these are analog amplifiers) have a built in gain of 2 to compensate for the loss.

We can easily setup our test circuit to observe the operation described. Add a 50 ohm resistor to the end of the coax cable and attach probes to testpoint_1 and testpoint_2.

6. Make a measurement with the cursors to determine amplitude of the signals at both testpoint_1 and testpoint_2. The amplitude should be about $Vdd/2$. The signals should look the same with the one at testpoint_2 being delayed by propagation down the coax. If your setup is correct, you should see something like Figure 9 below. Capture and include the oscilloscope picture of your measurements.

If R1 is set to zero ohms, it should be obvious that a full amplitude incident wave would be launched into the transmission line. With Rt at 50 ohms, no reflection would occur and a full-sized waveform would be received at the far end. This would be called a *parallel terminated* line which finds widespread usage.

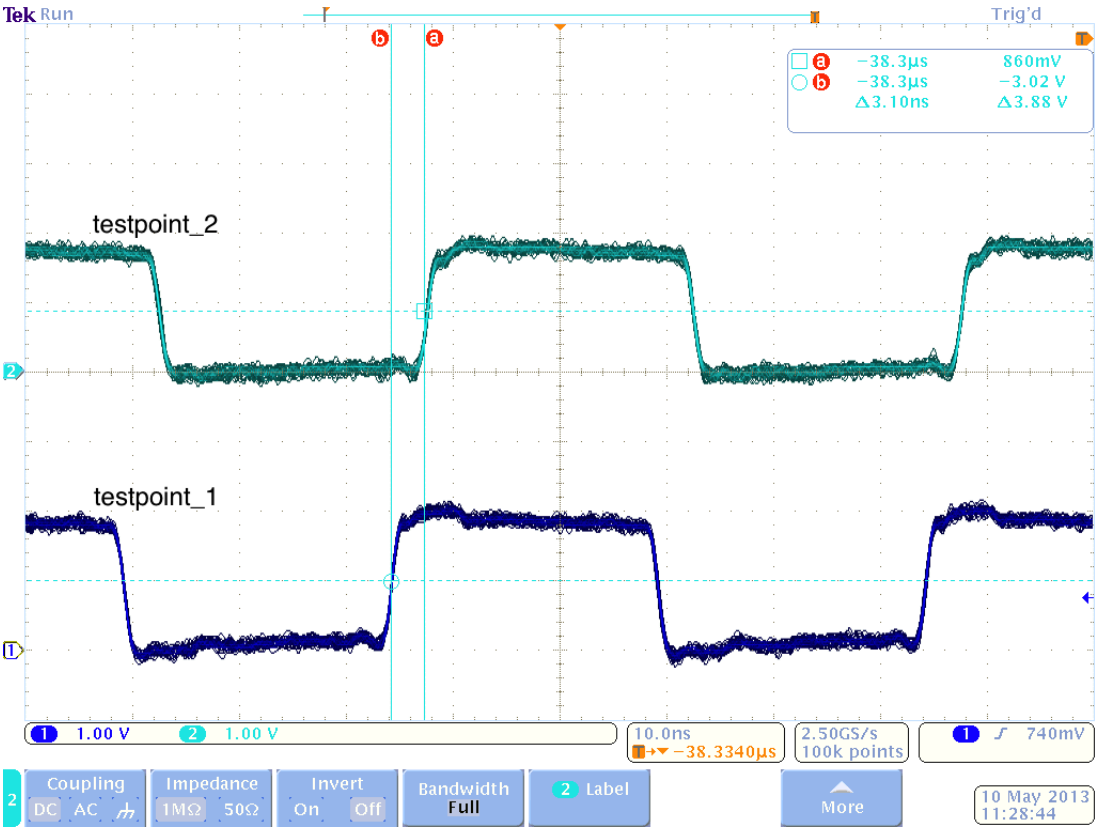


Figure 9: Double Terminated Transmission Line

Notes

- Keep decoupling capacitor and signal leads short.
- Don't include the Tek "waveform inspector" window in your pictures.
- Waveform measurements should fill at least one-half the scope screen. Otherwise they are too small to be of use.

Grading

Deliverable	**Grade Weighting**
Demonstrable, well built, working circuit	30%
Open Ended, Source Terminated	
#1, Measurement of round trip delay	10%
#2, Calculations and explanation of delay	15%
#3, Measurement of the Vdd/2 step	10%
Shorted End, Source Terminated	
#4, Measure of positive pulse with	10%
#5, Calculations and explanation of delay	15%
Double Terminated	
#6, Amplitude measurement	10%
Poorly formatted writeup	-10%
Can't make measurement from scope picture	-20%
Incorrect scope reading	-20%
Can't read scope settings	-20%
Prototype circuit is obviously wrong	-40%
Late, up to one week	-20%

Table 1: Grading Metrics