1. V_{dd} Anomaly #1 is a sudden drop in V_{dd} supplied to the driver. This is due to the L_{Vdd} inductor limiting the current available to the driver. When the driver is current limited by the inductor, it cannot launch as big of an incident wave.

As time goes on, the current through the inductor begins to increase allowing the edge to eventually reach V_{dd}. The edge of the incident wave however, follows V_{dd} pin almost exactly as the inductor current increases.

Voltage at V_{dd}-pin droops because of the direction of current flow through the inductor. $V_{dd} - V_{dd\text{-}pin}$ is a positive value which substracts directly from the voltage supplies to the driver.

V_{dd} Anomaly #2 is a result of the "inductive kick back" of the L_{VDD} inductor. Near the end of the first pulse, the current has reached a steady state value through the inductor. The current stays steady because of the parallel termination.

When the output buffer switches its output to a logic low state, almost no current is needed from V_{dd}. In a short period of time, the L_{VDD} inductor sees a current change and produces a reverse polarity voltage in an attempt to maintain the previously flowing current. Remember that the inductors nature is to oppose changes in current. We thus see a large positive spike in V_{DD}-pin.

(Note: Ringing is evident in the simulation on V_{dd}. This is most likely due to resonant behavior between capacitance at V_{dd}-pin and the 100nH inductor.)