4. a) A source series resistor of about 45 ohms gives a $\frac{V_{dd}}{2}$ "shelf" on the rising and falling edges. Given that the Z_0 of the line is 50Ω, the R_{out} of the buffer is about 5Ω.

b) +/- 10% of 3.3v is 3.63v + 2.97 volts

One value pair found was $L_{cap} \approx 0.5nH$ with $C_{VDD} = 100nF$. Decreasing C_{VDD} to 10nF still keeps the over + undershoot to < 10%

c) For a fixed decoupling capacitor size, a series terminated line has advantages. First, the incident current launched into a T-line is less. Thus the capacitor has to supply less current to the driver and is able to keep V_{DD} more stable.

Since the initial current is less, the V_{DD} capacitor can have more parasitic lead capacitance without causing problems. This may allow for a more relaxed capacitor placement or even a cheaper capacitor to be used.