9. a) For circuit (a), initial peak current would be

$$\frac{V_{dd}}{R_{src}+Z_0} \text{ or } \frac{V_{dd}}{2Z_0}$$

for circuit (b) initial peak current would be

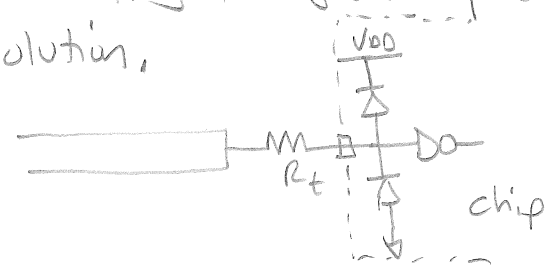
$\frac{V_{dd}}{Z_0}$; obviously the higher of the two

b) for (a) steady state current is ≈ zero as the CMOS input receiver has very high input resistance

For (b) steady state current is $\frac{V_{dd}}{R_t}$

c) If the effective on-resistance of N-channel transistor in (a) was equal to Z_0, no external terminating resistor would be needed

d) It would not work as the input resistance of the CMOS gate is very high, the resistor is essentially not connected to anything. It could work somewhat as the severe overshoot would be terminated through the protection diodes. Still not a correct solution.



e) The input buffer has no DC bias, it is floating.
- It could work if the pulses applied to the gate are short and have fast rise times.