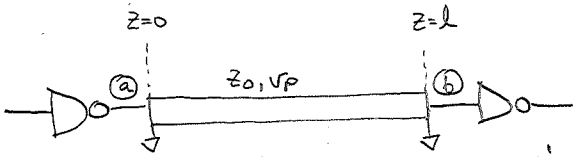
Heuristic Determination of T-line Environments
(not exact science... "it depends")

First look at the primarily digital environment

Our question is answered by looking at:
"rise time" versus "flight time"
t_R, t_F vs t_d

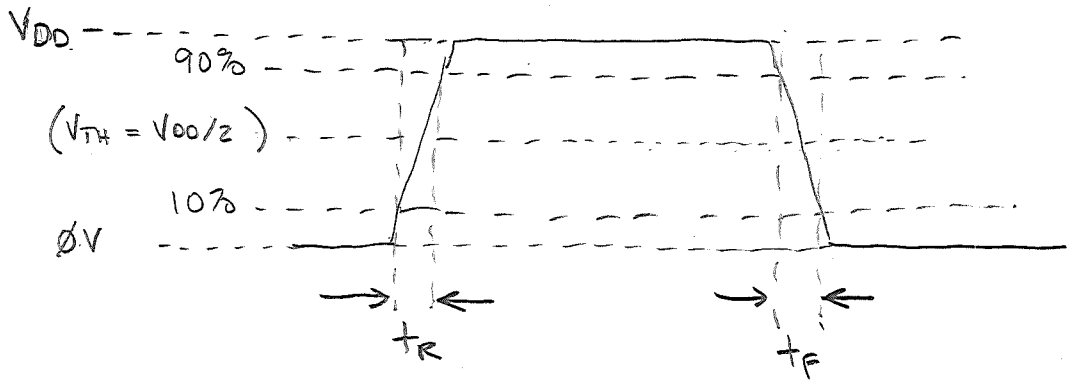


Flight time, t_d: how much time it takes to go from ⓐ to ⓑ

$t_d = \frac{l}{v_p}$

Flight time is the time it takes for the signal to traverse the signal path (one-way). We represent it as t_d. (Sometimes t_F)
(confused with fall time)

Rise Time (or Fall Time) t_r or t_f



(Note: for most CMOS circuits $t_r \approx t_f$ but not always.)

normally measured @ 10%, 90%

Heuristic Determination... (cont)

Wait a minute, what happened to frequency + wavelength?

Is there some relationship between t_{rise}, t_{FALL} and frequency?

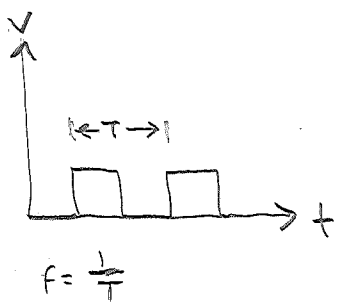
→ Yes!

Remember: Fourier Series Approximation for periodic Square wave?

$$f(x) = \frac{1}{2} + \sum_{k=1}^{\infty} \frac{2}{(2k-1)\pi} \sin((2k-1)x)$$

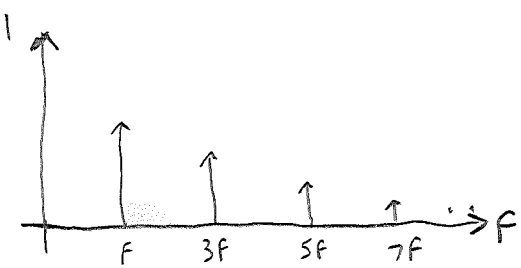
Ah yeah! A square wave is formed by summing an infinite number of sine waves from the odd harmonics of a fundamental frequency. f, 3f, 5f...

$$f(x) = \frac{1}{2} + \frac{2}{\pi}\sin(x) + \frac{2}{3\pi}\sin(3x) + \frac{2}{5\pi}\sin(5x) \ldots$$



time domain

⟹



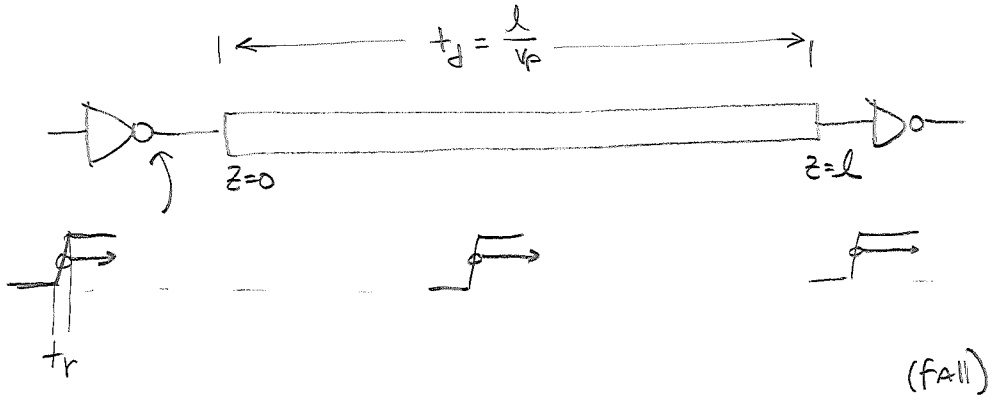
frequency domain

...So, sharp edged square waves contain very high frequency components.

...And edges with greater t_{rise} + t_{FALL} have fewer high frequency components.

Rule of thumb: most energy is at frequencies below $\frac{0.5}{t_{rise}}$ (Tektronix: $.35/t_r$ for probes)

Rise Time versus Flight Time



To behave as a lumped circuit, the rise time of the driver must be slow enough such that a point on the edge is seen everywhere on the line at very nearly the same time.

This is congruent with our statement that lumped circuits "see" voltage or current changes simultaneously throughout the circuit.

A fast rising edge is equivalent to a rapid phase change.

Heuristic Determination ...

- Digital Domain

Rise Time vs Flight Time

Compare the faster of (t_{rise}, t_{FALL}) with the one way propagation delay through the signal path (AKA "Flight time") $t_{delay} = \frac{\text{length of path}}{v_p}$

For CMOS IC's (and most others)

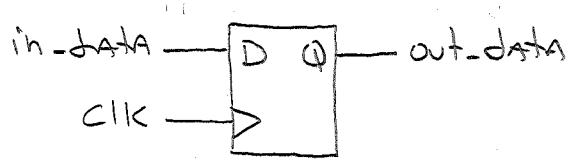
If $t_{rise} > 6 t_{delay}$; lumped circuit

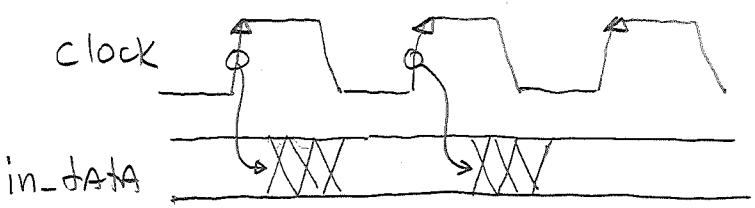
If $t_{rise} < 2.5 t_{delay}$; not lumped circuit (T-line scenario)

In between those values, it depends.

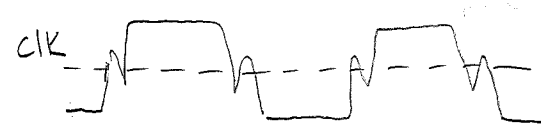
- Data or Clock signal
- Variation of temperature, voltage, process variations

Flip-flop clock inputs must be monotonic. The "D" input is far more forgiving.

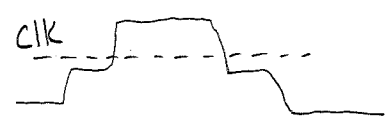




rising edge of clock causes data to be propagated forward



double clocking error



hold time failure

A pretty fast CMOS inverter

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu A$	0.8 V to 2.7 V	$V_{CC} - 0.1$			V
		$I_{OH} = -0.7$ mA	0.8 V		0.55		
		$I_{OH} = -3$ mA	1.1 V	0.8			
		$I_{OH} = -5$ mA	1.4 V	1			
		$I_{OH} = -8$ mA	1.65 V	1.2			
		$I_{OH} = -9$ mA	2.3 V	1.8			
V_{OL}		$I_{OL} = 100\ \mu A$	0.8 V to 2.7 V			0.2	V
		$I_{OL} = 0.7$ mA	0.8 V		0.25		
		$I_{OL} = 3$ mA	1.1 V			0.3	
		$I_{OL} = 5$ mA	1.4 V			0.4	
		$I_{OL} = 8$ mA	1.65 V			0.45	
		$I_{OL} = 9$ mA	2.3 V			0.6	
I_I	A inputs	$V_I = V_{CC}$ or GND	0 to 2.7 V			±5	μA
I_{off}		V_I or $V_O = 2.7$ V	0			±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V			10	μA
C_i		$V_I = V_{CC}$ or GND	2.5 V		2.5		pF

(1) All typical values are at $T_A = 25°C$.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V ± 0.1 V		$V_{CC} = 1.5$ V ± 0.1 V		$V_{CC} = 1.8$ V ± 0.15 V			$V_{CC} = 2.5$ V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	4.8	0.7	3.3	0.5	2.9	0.5	0.8	1.5	0.4	1	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V ± 0.15 V			$V_{CC} = 2.5$ V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.6	1.4	2.5	0.5	2	ns

These are propagation delays not rise & fall times.

But, you can be sure t_{rise} & t_{FALL} are way less than t_{pd}.

Learn to read data sheets

Operating Characteristics

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V	$V_{CC} = 1.5$ V	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	16	17	17	17	19	pF

Heuristic Determination:....

Most CMOS ICs exhibit $t_r \approx t_f \approx 1.0 - 2.5\,ns$. (AC, VHC Families) (< 1μm)

Typical PCB is FR-4 fiberglass with velocity of prop. ≈ 0.45c

Remember that $V_p \approx \frac{c}{\sqrt{\epsilon_r}}$; FR-4 $\epsilon_r \approx 4.7$ (FR-4 : Fire Resistant, fiberglass epoxy laminate)

Example: How long can the interconnect be at the output of a 74AUC04 when placed on a PCB with $V_p = 0.45c$ and be confidently treated as a lumped element?

Shooting for $\frac{t_r}{t_{delay}} > 6$; so

$$\frac{0.5 \times 10^{-9}\,s}{\frac{l\,m}{0.45c\ m/s}} > 6$$

$$\frac{(0.5 \times 10^{-9}\,s)\,0.45\,(300 \times 10^6)\,\frac{m}{s}}{l\,m} > 6$$

$$l_m = (0.5 \times 10^{-9}\,s)\,0.45\,(300 \times 10^6)\,\frac{m}{s}\,\left(\frac{1}{6}\right)$$

$\underline{l = 11.25\,mm \text{ OR } \approx 0.4''}$ (confidently lumped)

if $\frac{t_r}{t_f} > 2.5$.... $\underline{l = 27\,mm \text{ OR } \approx 1.0''}$ (better be careful)

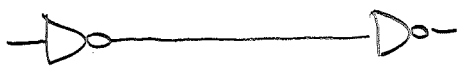
Heuristic Determination...

Slower CMOS parts (μCs) can typically drive $\approx 6''$ traces or wires without problems.

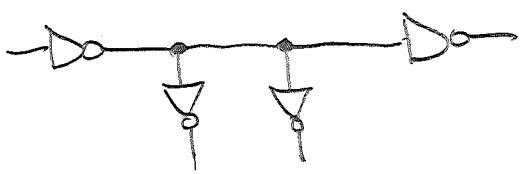
Given standard FR-4 PCBs, a quick judgement can usually be made by knowing the logic family, the length of the trace and the topology of the trace.

* Note that the preceeding rules of thumb only work for point-to-point connections with proper drivers receivers + possibly terminations.

pt. to point:



<u>not!</u> point to point:

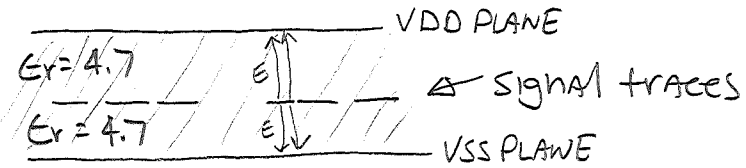


{this can be a bear to make work!}

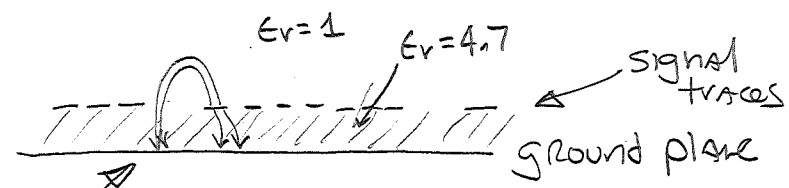
? What would the impact be if we simply treated all interconnect as if it was a transmission line?

Be careful with assumptions of t_r + t_f. They vary with V_{DD}, temperature + vendor lot. 2:1 variations are possible. "When it doubt; scope it out."

Flight time on a PCB is dependent on ϵ_r (typ 4.7) and the layer the trace is on. $v_p = \frac{c}{\sqrt{\epsilon_r}}$



All of E field is contained within the ϵ_r of the board. (slower traces)



part of E field is in the FR-4 $\epsilon_r \approx 4.7$, part of E-field is in air. Effective ϵ_r is somewhat different + is lower. (faster traces)

To summerize, "T-line or not" in the digital environment depends on:

- rise/fall time of the driver
- velocity of propagation of the medium
- physical length of the medium

} "electrical length", (A time or phase angle)

Signal t_r as a function of t_d (flight time)