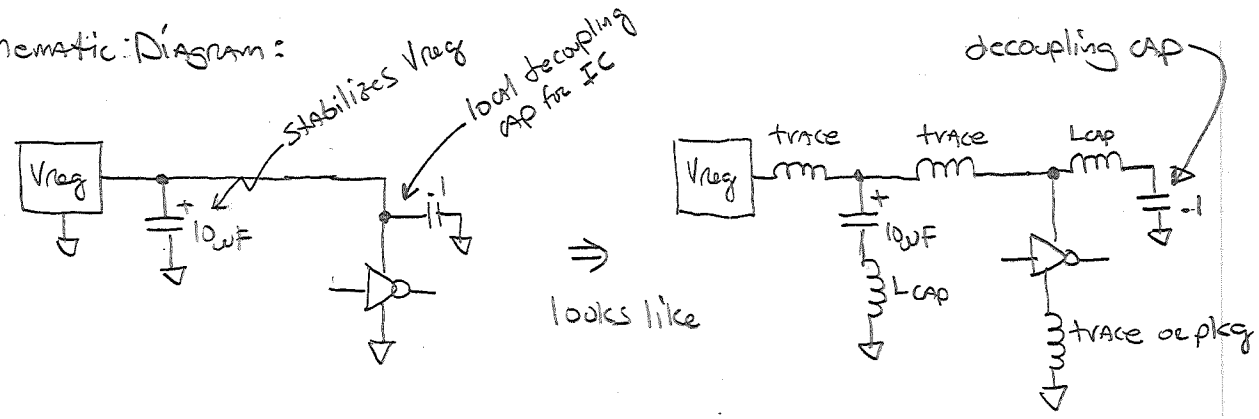
The T-Line Neighborhood – Power Supply

The power supply connection must be considered as part of the signal chain for digital IC's.

When the P-channel transistor turns on – it connects VDD to the output pin
N-channel " " " " " Vss to the output pin.

If VDD or Vss are "dirty" or they cannot support the current required, it will be apparent on the output pin.

Schematic Diagram:



The electrolytic capacitor at the regulator provides "bulk" decoupling and "pole setting for the voltage regulator. It is usually physically + electrically to far away to provide current rapidly to the IC.

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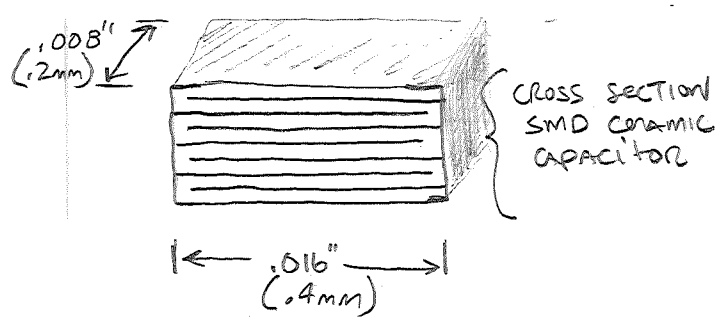
"Decoupling" capacitors decouple the IC from the inductance leading to the low impedance power source. It does so by providing a fast, local source of current to launch edges and support internal operation of the IC.

VDD or Vss traces can be long enough to present as T-Lines to power pins. A 0.125" trace on .062 board is about 50Ω. This is an extremely wide trace. Would you want to power your IC's through a 50Ω resistor?!

For decoupling capacitors to be effective, inductance to the capacitor must be minimized. This is done by using physically small capacitors and short leads. SMD chip caps or ceramic disk caps are best.



0402 chip cap
extremely low inductance

Capacitor internal or lead inductance is part of equation but physical placement is also critical.

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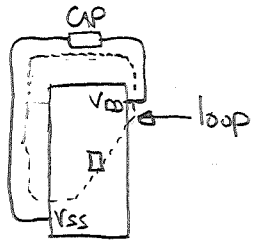
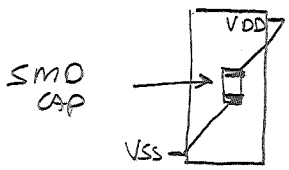
IC packages that have power pins on the package corners are the worst performers.



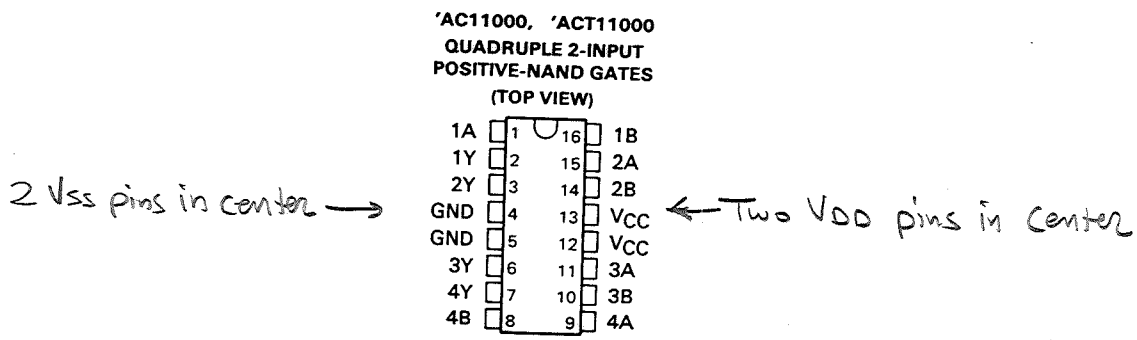
In a coiled wire, the larger the loop, the greater the inductance.

The complete loop must be considered, VDD to CAP to VSS.

A much better solution would be a SMD CAP on the bottom side of the board. The loop area is greatly reduced.



An extreme solution was TI's AC11000 family with "center VDD VSS" pins.



2 SMD caps could be placed directly underneath the package VDD + Vss pins.
Technically excellent, a failure in the marketplace.

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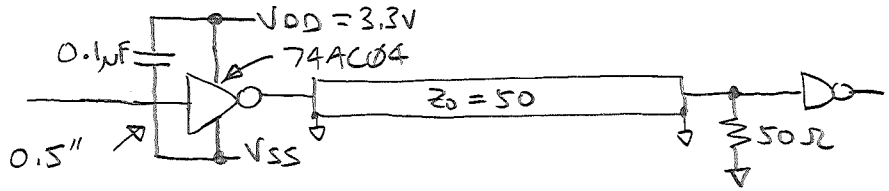
If leaded decoupling capacitors are used, lead length must be minimized

Imagine:



0.1μF cap, each lead 0.5", leads have dia of .01".

$L = 5.08\,l\left[\ln\left(\frac{4l}{d}\right) - 1\right]$; l = length, d = dia in inches, L in nH

$= 5.08(1)\left[\ln\left(\frac{4}{.01}\right) - 1\right]$ (1" total length)

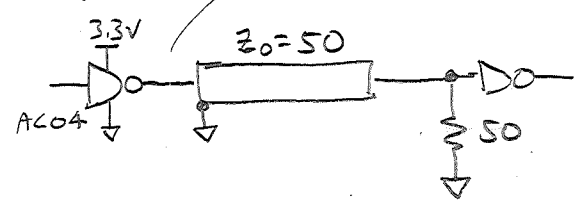
$= \underline{25\,nH}$

diminished rise and fall time since T-line is being charged through the inductance of the capacitor leads

$V_L = L\,di/dt$; let's compute the effect of lead inductance

$\frac{di}{dt} = \frac{\frac{3.3}{50}}{2ns}$ { going from 0 to 3.3V into 50Ω line { it does so over about 2ns

$V_L = (25\times10^{-9})\left(\frac{70\times10^{-3}}{2\times10^{-9}}\right) = \underline{\underline{0.88V}}$



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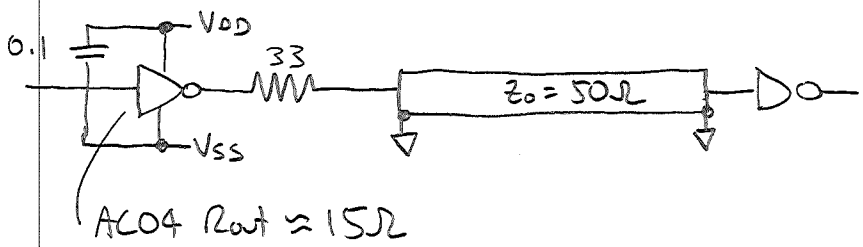
What if we terminated at the source? Is this better? Any advantage?



now, $\frac{di}{dt} = \frac{\frac{3.3}{83}}{2ns}$ { series, source termination is easier to drive!

$V_L = (25\times10^{-9})\left(\frac{40\times10^{-3}}{2\times10^{-9}}\right) = \underline{\underline{0.5V}}$ { much better, but pretty nasty! shorten the leads!

So, where & how we provide termination, can make a big difference in performance.

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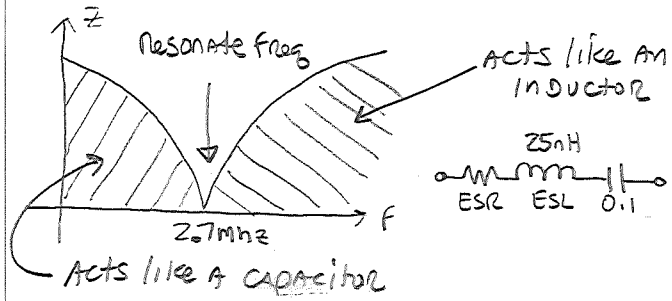
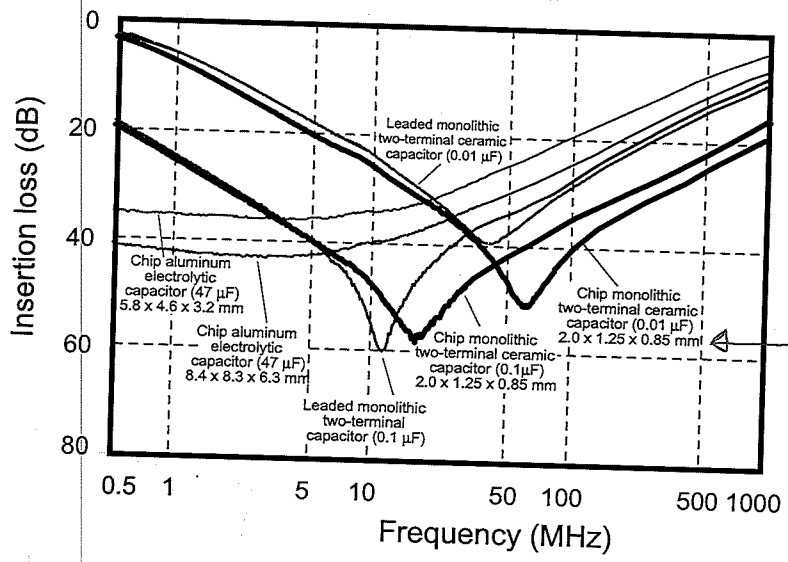
The impedance of a 0.1uF ceramic capacitor with 0.5" leads:



At resonance: $f = \frac{1}{2\pi\sqrt{LC}}$

For 0.1uF cap, 0.5" leads

Resonates @ 2.7Mhz, beyond this freq, its looking more & more like an inductor than a cap.



note higher self-resonant frequencies of ceramic SMD caps

0805 package