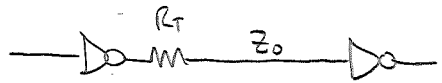
Termination Strategies

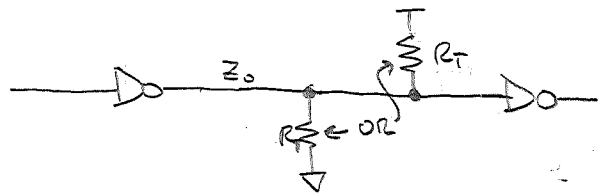
- Source, [series] Termination



$R_T = R_{out} - Z_0$

+ only one extra component
+ adds no DC load
+ lowers instantaneous current requirements
+ less crosstalk induced

- Parallel [load end] termination

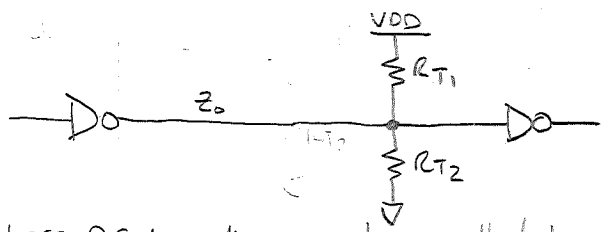


$R_T = Z_0$

- slower edge rate due to DC loading

+ can terminate to V_{DD} or V_{SS} (flexibility)
+ can be used with open drain drivers
+ R_T is easy to determine (only Z_0 dependent)
+ only one component
- DC power is dissipated in R_T
- needs decoupling if terminated to V_{DD}

- Thevenin Termination

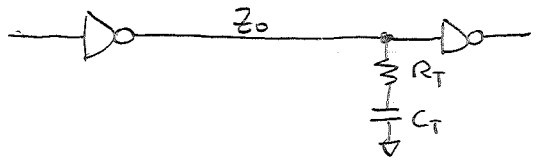


$R_{T_1} \| R_{T_2} = Z_0$

+ Less DC load than simple parallel termination
- must take care with DC levels to avoid linear operation of CMOS receivers (tri-state bus)
+ R_{T_1} + R_{T_2} can be chosen to "help" unbalanced R_{OUT} output buffers
- slower edge rate due to DC load
∘ usually seen on older TTL ckts

Termination Strategies

- AC termination

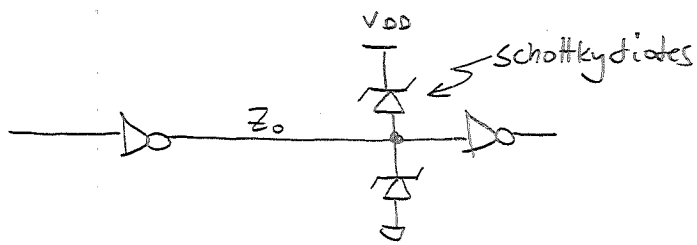


$R_T = Z_0$

[A number of equations exist for determining C_T. These form a good starting point only. Basically select C_T big enough to terminate the edge. Typical values are ≈ 50-100pF.]

+ behaves much like parallel method
+ R_T chosen ≈ Z_0
- C_T can be difficult to optimise
+ No DC power dissipation
+ full noise margins available
- can lead to timing problems
+ good for clock signals
- data pattern dependent delays

- Diode Termination



+ Don't need to know Z_0
+ Diodes can be placed anywhere reflections are present.
- need to use fast, low V_F diodes
- not really a matching or termination strategy.