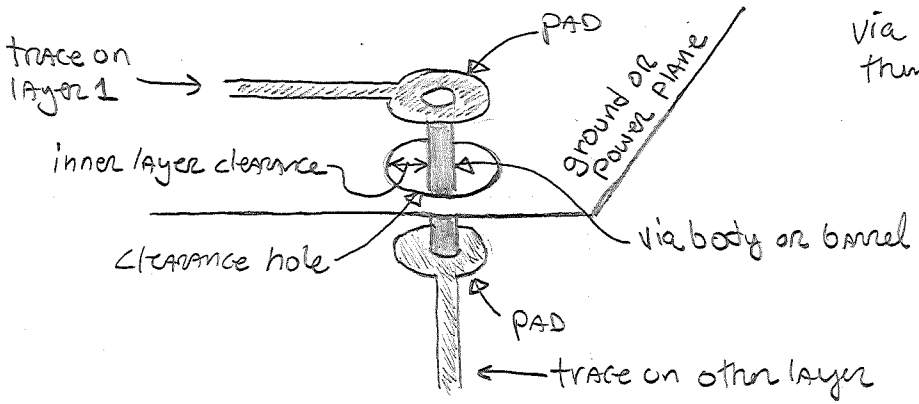
The T-Line Neighborhood - PCB Models

A VIA is a metal barrel in a PCB used to connect traces on different layers.



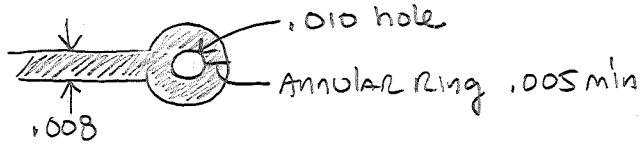
Via holes are first drilled then plated through

Vias create a parasitic capacitance to inner planes (ground or power)

The smaller the via, the less capacitance

The current limits on via size are ≈ .008 hole while .010 is typical

typical via and trace ⇒



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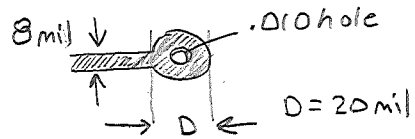
If we assume that vias have pads on inner layers also, the capacitance of a via is:

$$C_{via} = \frac{1.41\,\epsilon_r\,T\,D_{PAD}}{D_{clear} - D_{PAD}}$$; where

D_{PAD} = diameter of pad (in)
D_{clear} = diameter of clearance hole (in)
T = board thickness (in)
ϵ_r = dielectric constant of board
C_{via} = capacitance in pF

For our example (typical via) ⇒



$$C_{via} = \frac{1.41\,(4.7)(.062)(.020)}{(.024 - .020)} = 2\,pF$$ (small, 24 mil clearance hole)

$$C_{via} = \frac{1.41\,(4.7)(.062)(.020)}{(.030 - .020)} = 0.8\,pF$$ (large clearance, 30 mil)

Large clearances on inner layers produces a via with a smaller discontinuity

The primary effect of vias on <u>signal traces</u> is a slowing of the rise time due to the increased distributed capacitive loading that lowers Z_0.

For example, a string of vias occurring in a short distance could be a problem.

The T-Line Neighborhood - PCB Models

Vias also introduce a small inductive element that can significantly effect decoupling.
Back to the self-inductance of a wire (the via is now our wire)

$$L = 5.08h\left[\ln\left(\frac{4h}{d}\right) - 1\right];$$

where
L = inductance of via in nH
h = length of via (in.)
d = diameter of via (in.)

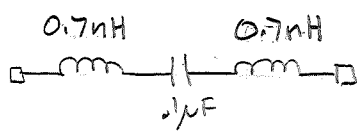
For a 10 mil via in .062 board:

$$L = 5.08(.062)\left[\ln\left(\frac{4(0.062)}{.01}\right) - 1\right]$$

$$= \underline{0.7nH}$$

Via diameter has little effect on the inductance
Via length (board thickness) makes the most difference

Since we will often have 2 vias, one for each end of the cap, we then have:



How will this effect the performance of our decoupling capacitor?

The T-Line Neighborhood – PCB Models

Assume we have an IC operating at 3.3V, sourcing a 1nS edge into 50Ω.
The voltage generated across both vias would be:

$$V_L = L\left(\frac{di}{dt}\right) = (1.4\times10^{-9})\left(\frac{\left(\frac{3.3}{50}\right)}{1\times10^{-9}}\right) = \underline{\underline{92\,mV}}$$

This is fine if only output is switching. What is 8 switch? $92mV \times 8 = \underline{\underline{736mV}}$

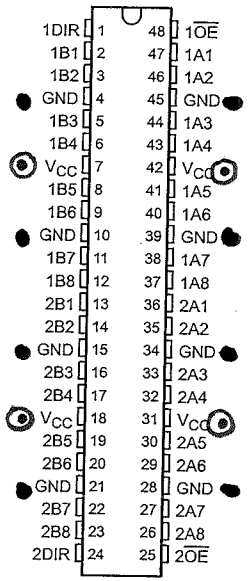
not ok!

SN54ALVTH162245, SN74ALVTH162245
2.5-V/3.3-V 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES331A – APRIL 2000 – REVISED APRIL 2002

- State-of-the-Art Advanced BiCMOS Technology (ABT) Widebus™ Design for 2.5-V and 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- High Drive
  - A Port = –12/12 mA at 3.3-V V_{CC}
  - B port = –32/64 mA at 3.3-V V_{CC}
- I_{off} and Power-Up 3-State Support Hot Insertion
- Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- A-Port Outputs Have Equivalent 30-Ω Series Resistors, So No External Resistors Are Required
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

SN54ALVTH162245 . . . WD PACKAGE
SN74ALVTH162245 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



8 Vss
4 VDD

4 outputs / VDD

description

The 'ALVTH162245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

```
Tline with one via (10mil via, .062 baord, 20mil pad)

*input source with 5ns delay, 1nS edges, 50ns pulse width, 101ns cycle time
Vin vin 0 3.3 PULSE(0 3.3 5e-9 1n 1n 50e-9 101e-9)
```

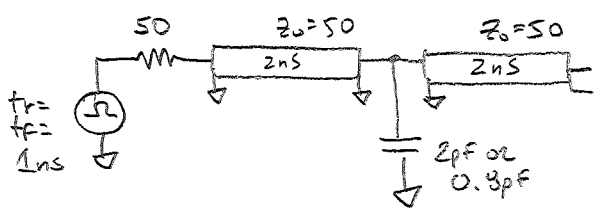
1nS edges

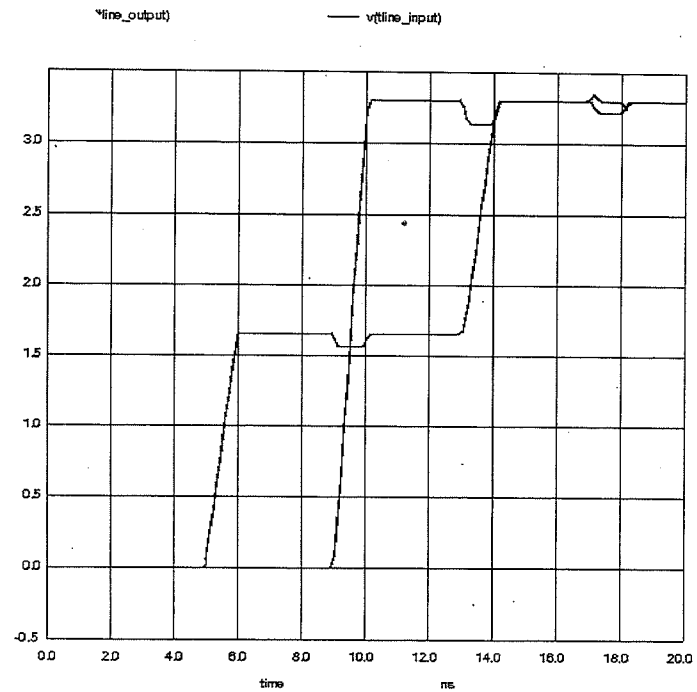
```
*source output impedance
rsrc vin tline_input 50

*transmission line number one, 50 ohm, 2ns electrical length
t1 tline_input 0 junction 0 z0=50 td=2ns

*transmission line number two, 50 ohm, 2ns electrical length
t2 junction 0 tline_output 0 z0=50 td=2ns

*cvia  junction  0 2pF
cvia  junction  0 0.8pF
```

24 mil clearance for via

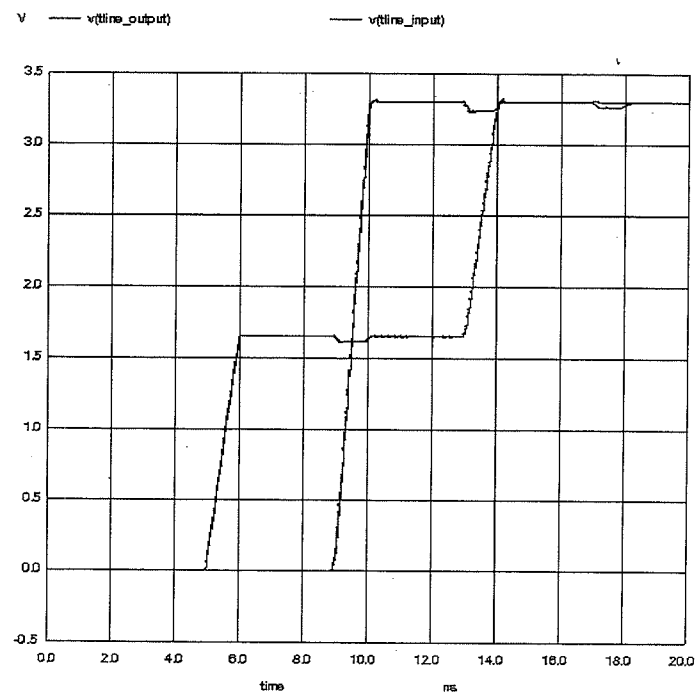
large clearance, 30 mil pad

```
.control
  op
  tran 100ps 101ns
  plot   V(junction) V(tline_output) xl 5ns 20ns


set hcopydevtype=postscript
set hcopypscolor=true
*set hcopydev=kec3112-clr

*color0 is background color
*color1 is the grid and text color
*colors 2-15 are for the vectors
set color0 = rgb:f/f/f
set color1 = rgb:0/0/0
set color2 = rgb:f/0/0
set color2 = rgb:f/0/f
hardcopy out.ps V(tline_input) V(tline_output) xl 0ns 20ns

.endc

.end
```





2pF via



0.8pF via